ISSN 2250-0987
Madhusudhan Dangeti et al, UNIASCIT, Vol 2 (3), 2012, 308-313

MINIMIZATION OF TRANSISTORS COUNT AND POWER IN AN EMBEDDED SYSTEM USING GDI TECHNIQUE

Madhusudhan Dangeti[1] , S.N.Singh[2]
[1,2] *National Institute of Technology Jamshedpur, India*

***Abstract*—Gate Diffusion (GDI) Input is a novel technique for low power digital circuit design in an embedded system. This technique allows reduction in power consumption, delay and area of the circuit. This technique can be used to reduce the number of transistors compared to convectional CMOS design. The performance of GDI is compared with CMOS and different other design techniques for several digital circuits.**

***Keywords*— CMOS, Gate Diffusion Input (GDI), Pass Transistor Logic (PTL) etc.**

I. INTRODUCTION

With the intensified research in low power, high speed embedded systems such as mobiles, laptops, etc has led the VLSI technology to scale down to nano regimes, allowing more functionality to be integrated on a single chip[7]. These efforts led to several different design techniques for digital circuits apart from traditional CMOS design style. GDI is one such new technique.

The PTL (Pass Transistor Logic) is most popular for low power digital circuits [7]. The main advantage of PTL over traditional CMOS design is: 1) high speed, due to low node capacitance, 2) low power dissipation, as a result of reduced number of transistors and 3) lower interconnect effect due to small area. But the implementation of PTL has two basic problems: 1) slow operation at reduced power supply as the threshold voltage drop across the single channel pass transistor results in low drive current, 2)the high input voltage level at the regenerative inverter is not Vdd, the PMOS device in the inverter is not fully turned OFF and hence direct path static power dissipation is significant.

GDI is a technique which is suitable for design of fast, low power circuits using reduced number of transistors compared to traditional CMOS design and existing PTL techniques. The aim of this work is to compare the GDI technique with other techniques; the results are compared with respect to traditional CMOS design style.

II. BASIC GDI CELL

The originally proposed GDI [5] is as shown in Fig. 1, which can be implemented using twin-well CMOS or SOI technology. The Fig. 2 shows the GDI cell that is compatible with standard CMOS process [1]. Some modifications in the standard CMOS inverter derives the basic GDI cell, where the sources of NMOS and PMOS are fed by input signals. GDI cell consists of 3 input terminals G, P and N.

Since it is not possible to implement all the functions of GDI, shown in Table I. Fig. 1 was proposed to implement in twin well CMOS or SOI technologies. It was believed that the bulk of both NMOS and PMOS should be connected to their source to minimize the body effect. The bulks of NMOS and PMOS are constantly connected to GND and Vdd respectively for GDI to be implemented in standard CMOS process. The influence of body effect is similar to originally proposed GDI. With the technology scaling the impact of transistor body effect on transistor threshold is highly reduced, making less relevant in the 65nm process and below [1].

The various functions that can be implemented with basic GDI cell, which consist of only 2 transistors is as shown in table I below. It can be seen that most of the logic gates can be implemented using the basic GDI cell which would require 4- 6 transistors using the standard CMOS process

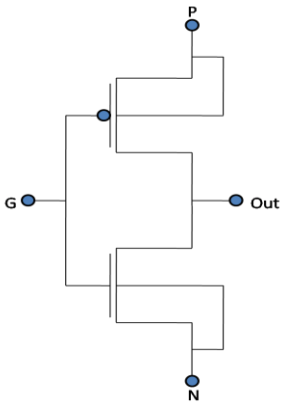


Fig. 1 originally proposed

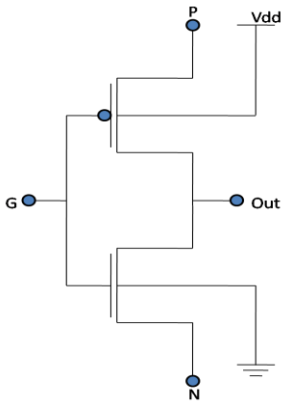


Fig. 2 compatible with standard CMOS process

,

TABLE I
FUNCTIONS THAT CAN BE IMPLEMENTED USING BASIC GDI CELL

N	P	G	Out	Function
0	1	A	A’	INVERTER
0	B	A	A’B	FUNCTION1
B	1	A	A’+B	FUNCTION 2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A’B+AC	MUX
B’	B	A	A’B+B’A	XOR
B	B’	A	AB+A’B’	XNOR

III. Advantages of GDI

From table I it can be seen that large number of functions can be implemented using the basic GDI cell. MUX design is the most complex design that can be implemented with GDI, which requires only 2 transistors, which requires 8-12 transistors with the traditional CMOS or PTL design. Many functions can be implemented efficiently by GDI by means of transistor count. Table 2 shows the comparison between GDI and the static CMOS design in terms of transistors count.

TABLE III
Comparison of Transistor count of GDI and Static CMOS

FUNCTION	*GDI*	*CMOS*
INVERTER	*2*	*2*
FUNCTION1	*2*	*6*
FUNCTION 2	*2*	*6*
OR	*2*	*6*
AND	*2*	*6*
MUX	*2*	*12*
XOR	*4*	*16*
XNOR	*4*	*16*
NAND	*4*	*4*
NOR	*4*	*4*

It can be seen from table II that using GDI technique AND, OR, Function1, Function2, XOR, XNOR can be implemented more efficiently. However to implement NAND, NOR it requires 4 transistors as that in Static CMOS design. NAND and NOR the universal logic gates, any Boolean Function can be implemented using these gates, are most very efficient and popular with static design style. Function1 and Function2 are universal set for GDI, and consists of only two transistors, compared to NAND and NOR. These functions can be used synthesize other functions more effectively than NAND and NOR gates [2].

IV. Operation Analysis of GDI Cell

Low swing of output signals is the problem in the PTL technique due to threshold drop across the single channel pass transistor, additional buffering circuitry is required to avoid this problem. To understand the analysis of low output swings in GDI consider the analysis of Function1. Table III shows the set of logic states and functionality of Function1.As we know that PMOS provides strong 1 and week 0 at its output and NMOS provides strong 0 and week 1 at its output From Table III it can be seen that low swing of output occurs when A=0, B=0, in this case the output is threshold voltage of PMOS ($V_{Tp)}$. This for the transition of B=1 to B=0 when A=0. When B=1 the GDI operates as a regular inverter, which is widely used as a digital buffer for logic level restoration without the swing drop from previous stage.

TABLE III
Input Logic States, Functionality and Output Swing of Function 1

A	**B**	**Functionality**	**Output**
0	0	PMOS Transmission Gate	V_{Tp}
0	1	CMOS Inverter	1
1	0	NMOS Transmission Gate	0
1	1	CMOS Inverter	0

V. Comparisons with Other Logic Styles

A. Basic GDI Functions

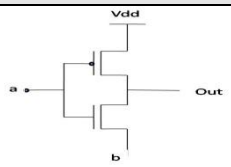
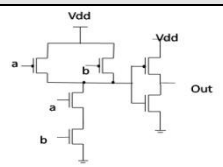
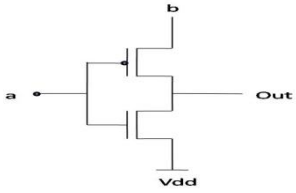
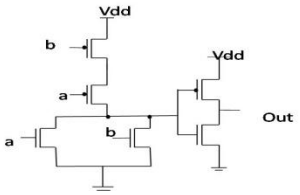
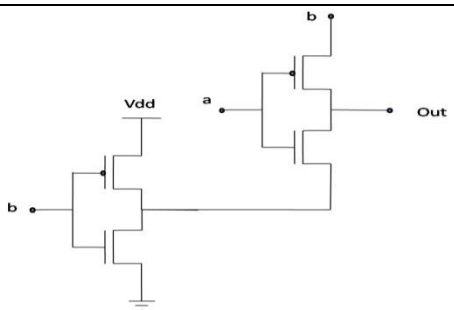
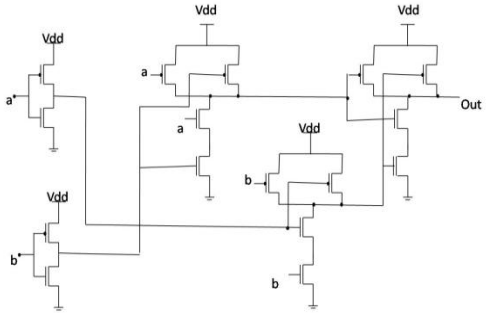
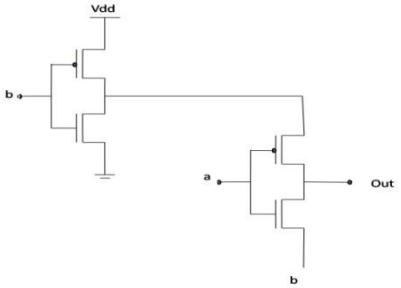
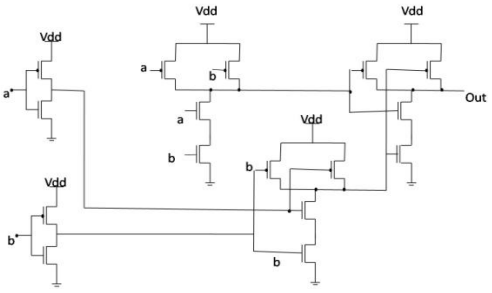
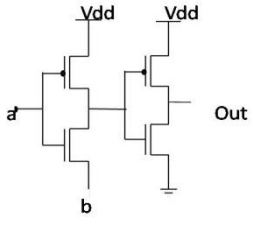
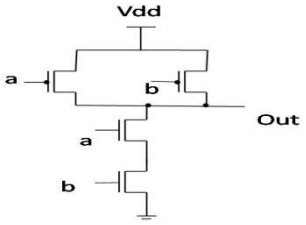
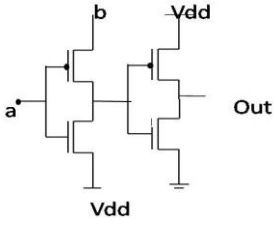
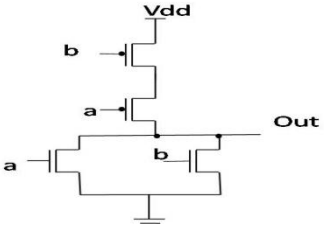
The circuits were tested in a 0.35-µm twin well CMOS process at 3.3v, 40MHz at 27 ^{degree} C [3, 5]. The comparisons were carried out for the GDI, standard CMOS, transmission gate and NMOS pass gate. For faith full comparisons of different techniques, comparisons are carried out from cells in series with buffers. GDI and transmission gate test setup has two basic cells followed by on one output buffer while the NMOS pass gate contains two buffers one after the other while the standard CMOS requires no buffers. Among all, the GDI requires minimum number of transistors. The average power consumed with reference to CMOS is listed in Table IV below. Table V shows the implementation of logic gates using GDI and standard CMOS logic to show transistor required.

TABLE IV
Percentage of Average Power Consumed by GDI, TG, N-PG with respect to CMOS

	GDI	**TG**	**N-PG**
MUX	71.8	90.3	95.5
OR	79.9	110	99.08
AND	75.3	90.3	88.26
Function 1	69	70.35	70.35
Function 2	74.2	77	68.67

From Table IV it can be seen that GDI technique consumes least percentage of power compared to CMOS and transmission gate logic and NMOS pass gate logic.

TABLE V
IMPLEMENTATION OF LOGIC GATES USING GDI TECHNIQUE AND CMOS

	GDI	CMOS
AND		
OR		
XOR		
XNOR		
NAND		
NOR		

B. Digital Circuits

Some of the digital circuits are implemented using 0.35µm CMOS process and the comparison of carried out between the standard CMOS logic and GDI Technique [8]. The percentage of power consumed with respect to standard CMOS and transistor count are mentioned in table VI below.

TABLE VI
PERCENTAGE OF AVERAGE POWER CONSUMED BY GDI WITH RESPECT TO CMOS AND TRANSISTOR REQUIRED ARE MENTIONED

Digital Circuit	Power consumed by GDI with respect to CMOS	Transistor Count GDI	Transistor Count CMOS
Ripple Carry Adder	70.4	72	168
Carry Bypass Adder	83.11	88	230
Carry Look Ahead Adder	73.02	80	208
Carry Select Adder	78.61	122	294
Binary Array Multiplier	81.67	296	600

C. 8-Bit Comparator

The 8-bit Comparator is implemented using 1.6µm CMOS process [4]. The comparison is carried for GDI technique, Standard CMOS process and NMOS pass gate. It is seen that GDI provides the best performance among the all, as it can be seen in Table VII, all 3 circuits are implemented 96 transistors.

D. 4-Bit Multiplier

The multiplier is implemented using 0.5µm CMOS technology with 3.3V supply voltage [4]. Comparison results are shown in table VIII. 26 transistors are used in GDI technique while 44 Transistors are used in standard CMOS.

TABLE VII
COMPARISON OF GDI, CMOS AND N-PG 8-BIT COMPARATOR

Logic Style	CMOS	GDI	N-PG
Power (mW)	1.82	1.41	3.87
Number of Transistors	96	96	96

TABLE VIII
COMPARISON OF GDI AND CMOS 4-BIT MULTIPLIER

Logic Style	CMOS	GDI
Power (mW)	1.265	0.3079
Number of Transistors	44	26

E. XOR Gate

XOR Gate is implemented using 180nm technology[2] and the comparison is done among Complementary Pass Transistor Logic(CPL), Dual Pass Transistors(DPL), standard CMOS and GDI Techniques and results are mentioned in table IX. Among all the implemented techniques GDI consumes least power and the least number of transistors. 23.93 micro Watts is consumed by standard CMOS, power consumed by different techniques is mentioned with respect to standard CMOS technique.

TABLE IX
COMPARISON OF GDI, CMOS, CPL AND DPL XOR GATE

Logic Style	CMOS	CPL	DPL	GDI
Percentage Power consumed with respect to CMOS	100	107.35	43.96	27.12
Number of Transistors	16	8	10	4

F. D-Flip Flop

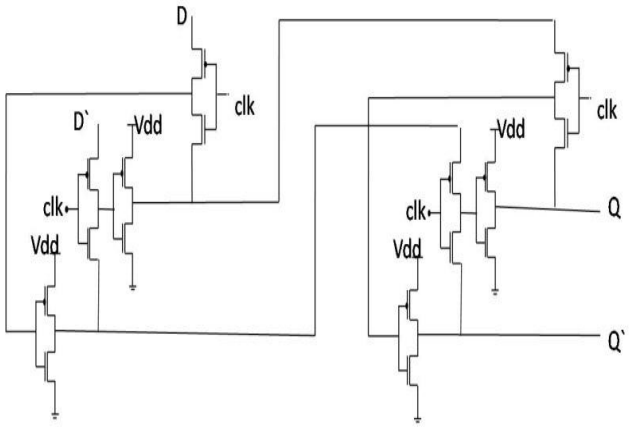


Fig. 3 D-Flip Flop Implementation using GDI

Fig. 3 shows the D-Flip Flop implementation using GDI. It is based on master slave connections of two GDI D-Latches. Each Latch consists of four basic GDI cells. To implement D Flip Flop it requires total of 18 transistors (16 shown in Fig. 3 plus 2 transistors to obtain D`). The circuit was implemented using 0.35µm and 0.18µm at 3.3 V and 1.8V respectively and its consumed 812.7uW and 151.7uW respectively [3].

VI. SIMULATION AND RESULT

Basic GDI Functions have been simulated using SPICE and the simulated outputs are show in Fig.4 below. These are the outputs of Basic GDI Cell without employing any level restoring circuits at their outputs. It can be seen that the outputs are within the range of noise margin to predict the correct output of the logic implemented by the Basic GDI cell. The simulation results of few functions as listed in Table I are shown in Fig. 4(a) to Fig. 4(f)

Fig. 4(a). Output of GDI Function1 (a`b)

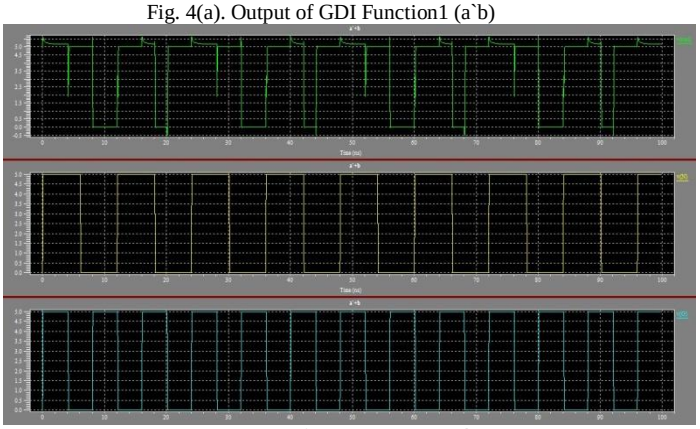


Fig. 4(b). Output of GDI Function2 (a`+b)

Fig. 4(c). Output of GDI AND Gate

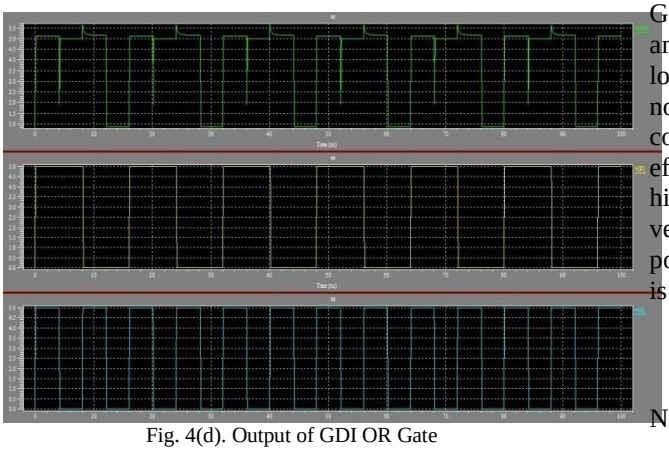


Fig. 4(d). Output of GDI OR Gate

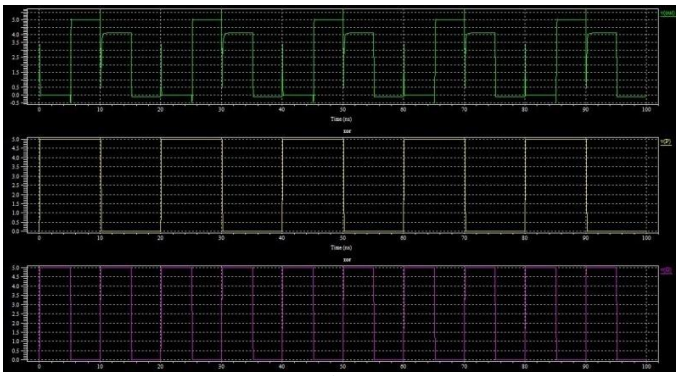


Fig. 4(e). Output of GDI XOR Gate

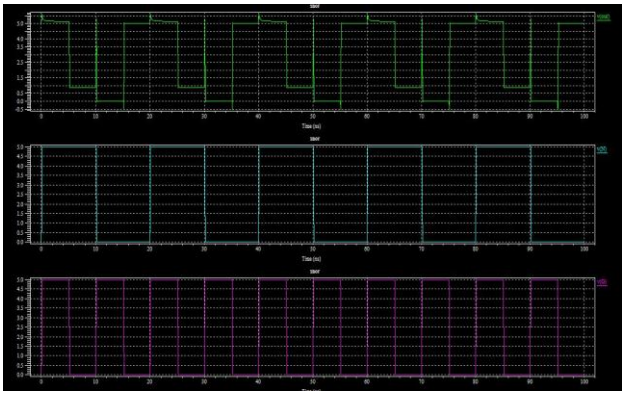


Fig. 4(f). Output of GDI XNOR Gate

VII. DISCUSSIONS

The simulated results confirm the functionality of all logical function as spitted in Table I. Power consumption as well as space reduction are among few major achievements in this new technique. The problem of threshold drop can be reduced by the proper sizing of transistors or by using level restoring circuits. The system may find its wide application in Embedded system ICs used in industrial as well as domestic applications

VIII. CONCLUSION

GDI technique is implemented for Basic Logic Gates and some Digital circuits. Comparisons are made among GDI, standard CMOS and some pass transistor logics. The analysis shows that the GDI technique is novel and an effective technique for reducing power consumption and the Transistor count which will effectively reduce the size of the chip. GDI will allow high density of Fabrication as now a day's chip area is very important parameter. With respect to chip area, power consumption and transistor count, GDI technique is significantly advantageous over other techniques.

ACKNOWLEDGEMENT

The work has been carried out in VLSI laboratory of National Institute of Technology Jamshedpur .

REFERENCES

[1] Arkadiy Morgenshtein, Idan Shwartz ,Alexander Fish, "Gate Diffusion Input(GDI) Logic in Standard CMOS Nanoscale Process", 26th convention of Electrical and Electronics Engineers, Israel,IEEE 2010.

[2] Atul Kumar Nishad and Rajeevan Chandel, "Analysis of Low Power High Performance XOR Gate using GDI Technique", Conference, IEEE 2011

[3] A. Morgenshtein, A. Fish, I.A. Wagner, "An Efficient Implementation of D-Flip-Flop Using The GDI Technique", Proc. of ISCAS'04 Conference, Canada, pp. 673-676, May 2004

[4] A. Morgenshtein, A. Fish, I. A. Wagner, "Gate-Diffusion Input (GDI) – A power-efficient method for digital combinatorial circuits", IEEE Transactions on VLSI systems, vol.10, no. 5, October, 2002.

[5] A. Morgenshtein, A. Fish, I. A. Wagner, "Gate-Diffusion Input (GDI) – A Novel Power Efficient Method for Digital Circuits: A Design Methodology", 14th ASIC/SOC Conference, Washington D.C., USA, September 2001.

[6] A. Morgenshtein, A. Fish, I. A. Wagner, "Gate-diffusion input (GDI) – a technique for low power design of digital circuits: analysis and characterization", Proc. IEEE International Symposium on Circuits and Systems, vol. 1, pp. 477-480, Arizona, USA, May 26-29, 2002.

[7] N. Weste, K.Eshraghian, "Principles of CMOS Digital Design", Addison-Wesley.pp.304-307.

[8] Padmanabhan Balsubramanian, Johince John,"Low Power Digital Design using modified GDI", IEEE, 2006

Biographies

Dr S.N. Singh had completed doctoral PhD degree at the Department of Electrical Engineering, National Institute of Technology Jamshedpur (India). He obtained his B.Tech degree in Electronics and communication engineering from BIT Mesra (A Deemed university), Ranchi - Jharkhand (India) in 1979/80. Presently his area of interest is *solar energy conversion technology*. He had published more than 50 papers in National and International journals based on his research work. He had remained *Head of Department of Electronics and Communication Engineering for* two terms and presently heading Govt. of India sponsored VLSI SMDP-II Project**.**

Madhusudhan Dangeti is pursuing his M.Tech degree in VLSI Design and Embedded Systems from National Institute of Technology Jamshedpur (India). He obtained his B.Tech degree in Electronics and communication engineering from S.R.K.R Engineering College, Bhimavaram, Andhra Pradesh (India) in 2010. His area of interest is *digital VLSI design*, *Embedded Systems.* He is associated with many projects in VLSI Design as applied to an industrial control system.