ARCHITECTURE OF SOFTWARE DEFINED RADIO USING DIGITAL SIGNAL PROCESSOR

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***Abstract*:**In considering the architecture of the radio device, whether mobile terminal or base station it simply divided into two areas. RADIO FRONT END ,RADIO BACK END .Radio front end is related to the radio frequency aspects both receiver and transmitter section , and hardware is the dominant element for the front end. Where as Radio backend is related to the signal processing functionalities, and hardware coupled with software as the dominant element of the back end. Software radio design begins at the antenna .Wideband antennas are needed to access multiple RF bands dynamically, sequentially or in parallel. Performance of the antenna and RF to digital conversion plays a key part in determining the capabilities of an SDR platform .At same time ,the flexible digital signal processing is what qualifies a radio as being a software –defined radio .Software radios employ a combination of techniques that include multi-band antennas and RF conversion. Wide-band A to D and D to A conversion and implementation of IF, base band and bit stream processing functions in general purpose programmable processors. A receive or transmit path in a software radio consists of high speed, wide dynamic range analog data converters, and digital converters, receive signal processors, and and transmit signal processor.

The RF front –end on the receive path performs RF amplification and analog down conversion from RF to IF. On the transmit path. RF front-end performs analog up conversion and RF power amplification[1].

Key words: Software Radio-Technic progress-Review-Reconfigurable circuit-Mobile service radio communication-Mobile station-Radio frequency-Baseband-Telecommunication regulation

1.INTRODUCTION:

The wireless networks are must to connect these systems. With the emergence of new standards and protocols has led to wireless communication development at a furious pace. High-speed wireless network of next generation are also expected to support multimedia applications. Existing technologies for voice, video, and data use different packet structures, data types, and signal processing techniques. Integrated services can be obtained with either a single device capable of delivering various services or with a radio that can communicate with devices providing complementary services. The supporting technologies and network that the radio might have to use can vary with the physical location of the user. The radio has to communicate and decode the signals of devices using different air interfaces to successfully communicate with the systems. to manage changes in network standards, protocols, services, and environments, the mobile devices require reconfigurable hardware that can support seamlessly multiple protocols, such as **IP** , **VoIP** and **MExE** . Such radios can be implemented efficiently using **software radio architecture** in which the radio reconfigures itself based on the system it will be interfacing with and the functionalities it will be supporting [2].

Software Radios are configurable hardware platforms that provide the technology for realizing the rapidly expanding third and future generation digital wireless communication infrastructure. As advancements in digital technology continue, the Communication industry continues to feel the impact of these advancements and the relationship between digital and communication technology strengths. As a result new digital technologies gain great exposure through the communication market. Now another change is possible, from digital hardware to digital software. The concept of the software radio is an embodiment of these two technologies. [3][4]

1.1Analog to Digital Converters Architecture: The basic components of an ADC are a sampling circuit, comparators, and encoding logic. These basic components can be linked in variety of ways to create different ADCs architectures [1][5].

1.1.1 Flash Analog to Digital Converter: The parallel ADC converts analog signal to digital form by simultaneously considering the relationship between the digital output code and the reference voltage across all allowable quantization levels. This basic structure exists for the Flash ADC is shown in figure 1.1 [1] [6]

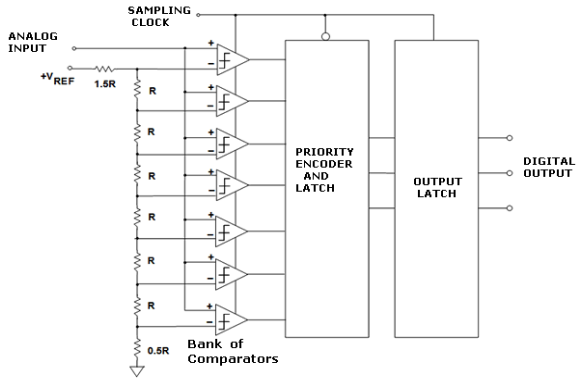

Figure 1.1: Three-Bit Flash (Parallel) Analog to Digital Converter

The Flash ADCs are also called as "parallel" ADCs. Flash ADC is the fastest type of ADC and use large numbers of comparators. An N-bit flash ADC consists of 2^N resistors and $2^N - 1$ comparators bank arranged as shown in Figure 1.1. Each comparator has a reference voltage from the resistor string, which is 1 LSB higher than that of the one below it in the chain. For a given input voltage, all the comparators below a certain point will have their input voltage larger than their reference voltage have a logic output "1", and all the comparators above that point will have a reference voltage larger than the input voltage have a logic output "0". The 2^N–1, comparator outputs therefore behave in a way analogous to a mercury thermometer, therefore the output code at this point is sometimes called as a "thermometer" code. Since the 2^N–1 data outputs are not really practical, so a decoder to generate an N-bit binary output processes them.

The input signal is applied to all the comparators simultaneously. So the thermometer output is delayed by only one comparator delay from the input, and the encoder N-bit output by only a few gate delays at the encoder. Therefore the process is very fast. In addition, the individual comparators provide an inherent "sample-and-hold" function, so theoretically a flash converter does not need a separate SHA (Sample-and-hold Amplifier), provided the comparators are perfectly dynamically matched. In practice, however, the addition of a proper external sample-and-hold usually enhances the dynamic performance of most flash converters because of the inevitable slight timing mismatches which occur between comparators.

Advantages of Flash ADC:

1. The Flash structure provides the fastest data conversion as compared to all possible architectures because only one analog stage is required.

2. Flash ADCs are easy to design in VLSI (Very Large Scale Integration) for small number of Bits.

Disadvantages of Flash ADC:

1. The flash converter uses large numbers of resistors and comparators and which limits the resolutions.

2. Area and power consumption of flash ADC increases exponentially with the number of bits.

3. Stable voltage source required because as the number of bit increases the voltage steps shrink

4. As the number of bit increases the number of comparators also increases, which results in increase of input capacitance and decreases analog bandwidth.

1.2 Digital to Analog Converter Architectures: The Digital to analog Converter (DAC) converts digital signal into analog signal. D/A conversion starts with a binary number as the input, and the output is a voltage step. It is not a true analog value that varies continuously; it is a discrete voltage that varies in steps. A D/A converter's output are always rounded to a voltage step or a discrete voltage value; therefore it is important to pick the right resolution for a D/A converter. The number of voltage levels of a D/A converter can be given by the number of bits that are used to represent the input binary signal [2][5].

Number of voltage levels = $2^{(\text{number of bits N})}$

The amplitude of the DAC output can be expressed as:

$$Analog\,Output = \frac{DigitalInputCode}{2^N - 1} \times Reference Input$$

2. ADC SPECIFICATIONS:

The wide variety of analog-to-digital converter applications leads to a large number of specifications for specifying the performance. These specifications includes the accuracy, resolution, dynamic range, offset, gain, differential non-linearity (DNL), integral non-linearity (INL), signal-to-noise ratio, signal-to-noise-and-distortion ratio, effective number of bits, spurious-free dynamic range, total harmonic distortion, effective resolution bandwidth, aperture delay, and aperture jitter. These specifications can be divided into two categories: [7]

1. Static specifications and,
2. Dynamic specifications

2.1 Static specifications:

a. Accuracy: Accuracy is the total error with which the A/D converter can convert a known voltage, including the effects of quantization error, gain error, offset error, and nonlinearities.

b. Resolution: Resolution is the number of bits N, which is output of the A/D converter. Resolution determines the size of the least significant bit (LSB), and thus determines the dynamic range, the code widths, and the quantization error [1]. The number of quantization levels is determined by the number of bits N used and is given by

Number of Quantization levels = 2^N .

For the uniformly distributed quantization levels, the ADC's resolution in terms of step size is generally represented by the symbol Δ. For a uniform distribution, the step size corresponds to the value of LSB and can be calculated by

$$LSB = \Delta = \frac{V_{FS}}{2^N}.$$

c. Dynamic Range: The dynamic range is the ratio of the smallest possible output i.e. (the least significant bit) to the largest possible output (full-scale voltage).

d. Offset Error: Offset error is the deviation in the A/D converter's behavior at zero input. The first transition voltage should be 1/2 LSB above analog ground. Offset error is the deviation of the actual transition voltage from the ideal 1/2 LSB.

e. Gain Error: Gain error is the deviation in the slope of the line through the A/D converter's end points at zero and full scale from the ideal slope of $2^N/V_{FS}$ codes-per-volt.

f. DNL and INL: These properties actually indicate the accuracy of a converter and include the errors of quantization, nonlinearities, short-term drift, offset and noise. The definitions of static linearity that is INL and DNL of A/D converters are indicated in the transfer curve of a converter shown in Figure 2.1. Integral nonlinearity (INL) sometimes called relative accuracy, is defined as the deviation of the output code of a converter from the straight line drawn through zero and full-scale excluding a possible zero offset. The nonlinearity should not deviate more than ± 1/2 LSB of the straight line drawn. This INL boundary implies a monotonic behavior of the converter. Monotonicity of an analog-to-digital converter means that no missing codes can occur.

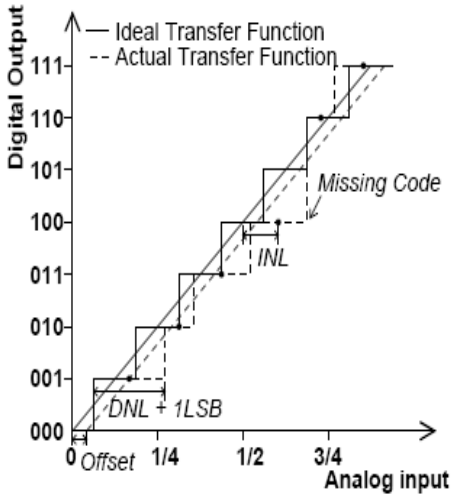

Figure 2.1: Transfer function of a 3-bit A/D converter [8]

Differential nonlinearity (DNL) is the deviation of the code transition widths from the ideal width of 1 LSB. Differential nonlinearity (DNL) error gives the difference between two adjacent analog signal values compared to the step size of a converter generated by transitions between adjacent pairs of digital code numbers over the whole range of the converter.

The DNL of ADC output Di can be written as,

$$DNL(D_i) = \left(\frac{V_{in}(D_i) - V_{in}(D_{i-1}) - V_{LSB}}{V_{LSB}} \right)$$

Where D_i and D_{i-1} are two adjacent digital output codes. There is a direct connection between the INL and DNL. The INL for output Dm can be obtained by integrating the DNL until code m. [9]

$$INL(D_m) = \sum_{i=1}^{m} DNL(D_i)$$

2.2 Dynamic specifications:

1. Signal-to-Noise Ratio: The quantization process in ADC introduces an error, which sets the limit for the dynamic range of an A/D converter. The quantization noise power (N_Q) can be calculated from mean squared error (MSE) signal is given as, [1] [9]

$$N_Q = \frac{V_{FS}^2}{12 \times 2^{2N}}$$

The zero mean uniformly distributed signals is input quantizer; the average signal power is variance of the input signal

$$P_x = \frac{V_{FS}^2}{12}$$

The signal quantization noise ratio (SQNR) is defined as the ratio of signal power to the noise power.

$$SQNR = \frac{P_x}{N_Q}$$

$$SQNR = 6.02N$$

The average SQNR for a sinusoidal signal can be obtained to be

$$SQNR = 6.02N + 4.77 - 10\log_{10}\eta \text{ dB}$$

If oversampling is used, which means that the sample rate F_s is much larger than the signal bandwidth B_S, the quantization noise is averaged over a larger bandwidth and the signal-to-quantization noise ratio becomes larger, written as

$$SQNR = \left(6.02N + 4.77 - 10\log_{10}\eta + 10Log_{10}(OSR) \right) \text{ dB}$$

Where the oversampling ratio OSR is given by,

$$OSR = \frac{F_S}{2B_S}$$

By doubling the OSR or F_S the SQNR improves by 3 dB. [1] [9]

2. Dynamic Range: To successfully process the desired signal, the ADC must accommodate interference. The wideband front-end may allow more interference. Software Radio implementations typically utilize a wideband front-end, so dynamic range of the selected ADC is a very important consideration in a software radio implementation. The dynamic range of a ADC can be calculated from the SQNR. The dynamic range of an ideal A/D Converter, assuming sinusoidal input signal is given as

$$DynamicRange_{ideal} = SQNR = 6.02 \times N + 1.763 \text{ dB}$$

The dynamic range of practical data converters will be affected by any distortion or noise the A/D Converter may introduce. The dynamic range of a practical A/D converter can be defined as

$$DynamicRange_{practical} = 10Log_{10}\left(\frac{\frac{V_{FS}^2}{12\eta}}{N_Q + N_{Thermal} + \sum_{K=1}^{N} P_K} \right) \text{ dB}$$

Where $N_{Thermal}$ is the thermal noise and P_K is the power in a harmonic, both introduced by the A/D converter.

3. Signal-to-Noise-and-Distortion Ratio (SINAD): The noise and signal both degrade the signal quality. The SINAD ratio is defined as the ratio of the signal power, Po to the sum of all the noise sources, N plus the distortion from the sum of the harmonics, Pi within the first Nyquist zone. [3]

$$SINAD = 10\log_{10}\left(\frac{P_O}{N + \sum_{i=1}^{\infty} Pi} \right) \text{ dB}$$

4. Effective Number of Bits (ENOB): The dynamic range of a practical A/D converter is less than the ideal A/D converter or it is equivalent to an ideal A/D converter using lesser number of quantization bits. Thus the dynamic range of a A/D converter can be expressed in terms of the effective number of bits (ENOB). The ENOB can be calculated as

$$ENOB = (SINAD - 1.763)/6.02$$

5. Total Harmonic Distortion (THD): The nonlinear processes create harmonics. These harmonics distort the signal and degrade the performance. The THD is defined as the ratio of the sum of the powers of the harmonics, P_i, i =1, 2, ------ ∞ to the power in the fundamental, Po. THD is given as

$$THD = 10Log_{10}\left(\frac{\sum_{i=1}^{\infty} Pi}{Po} \right) \text{ dB}$$

6. Intermodulation Distortion (IMD): The creation of harmonics due to mixing of two tones is

known as Intermodulation Distortion (IMD). For two tones with frequencies f_0 and f_1, then their IMD harmonics, H_i, can be calculated as

$$IMD(H_i) = mf_0 - nf_1$$

Where m, n = -∞ …, -2, -1, 0, 1, …∞.

7. Spurious-Free Dynamic Range (SFDR): Spurious-free dynamic range (SFDR) is the ratio of the input signal to the peak spurious or peak harmonic component. Spurs can be created at harmonics of the input frequency due to nonlinearities in the A/D converter, or at subharmonics of the sampling frequency due to mismatch. The dynamic range available in the presence of the spur is the SFDR of the A/D converter and can be calculated as [1]

$$SFDR = 10Log_{10}\left(\frac{P_O}{\max(P_i)}\right) \text{ dB}$$

8. Effective Resolution Bandwidth: Effective resolution bandwidth (ERBW) is the input-signal frequency where the SNDR of the A/D converter has fallen by 3 dB from its value for low-frequency input signals. [7]

9. Aperture Jitter: The average value of the spacing between clock pulses is equal to the desired sampling period, Ts; the instantaneous spacing between samples may vary greatly and unpredictably. The sample-to-sample uncertainty in the spacing between impulses is termed as aperture jitter τ_a. [1]

In communication system, aperture jitter causes uncertainty in the phase of the sampled signal, degradation of the noise floor of an ADC, and increases the possibility of ISI. These effects are directly proportional to the signals slew rate. The high frequency signals suffer more extensive signal quality reduction from aperture jitter than low frequency signals. The maximum input frequency for a given aperture jitter specification can be calculated as

$$f_{\max} \le \frac{1}{2^N \pi \tau_a}$$

Where N is the number of bits, f_{max} maximum input frequency.

3.1 Introduction to GSM:

The GSM (Global System for Mobile Communication) is second-generation digital cellular system. This system is worldwide accepted and one of the most popular system. Due to the popularity of this system, the service providers are yet not able to ignore the GSM services on the basis of economics. Hence the GSM specifications are considered for Software Defined Radio platform.

3.2 GSM-900 System Specifications: GSM is digital cellular wireless mobile communication system. For the primary band in the GSM-900 system specifications are given in Table 3.1:

Sr. No.	Parameters	Values
01	RF channel Spacing	200 KHz
02	Access Technology	TDMA/FDMA
03	Primary Use	Cellular
04	Frequency Bands [UHF Wa=25 MHz]	935-960; 890-915
05	Duplexing	FDD
06	Modulation	GMSK
07	Frequency Assignment	Fixed
08	Handset Power [max/Average]	1000/125 mW
09	Power Control MS-BS	YES-YES
10	Speech-Coding	RPE-LTP
11	Speech Rate (Kbps)	13
12	Speech Channel per RF channel	8
13	Channel bit rates (Kbps)	270.833
14	Channel Coding	½ rate Convolution
15	Frame Duration	4.615 ms

Table 3.1: GSM 900 System Specifications

3.2 Calculation of ADC Parameters:

The GSM operating constraints are listed in Table 3.2:

Channel Bandwidth	**200 KHz**
Received Signal Strength	**- 101 dBm**
Interference Strength	**- 13 dBm**
Total Signal Power	**- 13 dBm**
Front-end-Noise Figure	**3 Db**
ADC Sampling Frequency Fs	**100 Msps**
Maximum ADC Power	**2 dBm**
Safety Margin	**9 dB**
SNR for 2% BER	**6 dB**

Table 3.2: GSM-900 Operating Specifications.

Impact of Noise and Interference on Dynamic Range: The dynamic range requirements for a software radio's ADC are highly dependent on the environment in which the software radio is designed to operate and the waveform being implemented. Interference from in-band or channel noise may be significantly stronger than the desired signal. For channel noise only, selecting an ADC with sufficient resolution to discriminate between the desired signal and the noise. However, care must be taken to ensure that the interference neither over-ranges nor under-ranges the ADC. [3]

The required dynamic range is a function of the received signal power, interference power, and input noise for specific environment can be expressed as

$$DynamicRange_{required} = \max\left\{-10Log_{10}\left(\frac{C}{N_{T,C}+\sum_{K=1}^{N} I_K}\right),0\right\} + SNR_{\min}\ \text{dB}$$

Where C is the received signal power, $N_{T,C}$ is the total input noise power from thermal noise sources and channel noise, I_K interference power, and SNR_{min} minimum SNR.

When one interferer is significantly stronger than the other signals and the noise; then the dynamic range can be given as

$$DynamicRange_{required} = \max\{I_{\max}\,dBm - CdBm, 0\} + SNR_{\min}\ \text{dB}$$

where I_{max} is the power level of the strongest interferer.

Dynamic Range$_{required}$ = 88 dB.

Number of Quantization Bits (N):

The minimum number of quantization bits is required for an ideal ADC with the desired dynamic range can be determined by

$$N \geq \left(\max\{I_{\max} - C, 0\} + SNR_{\min} - 4.77 + 10Log_{10}\eta - 10Log_{10}OSR\right) \Big/ 6.02$$

Where η is the peak-to-average-power ratio of the signal and interference. η =2 for sinusoidal input signal.

Oversampling Rate (OSR): The oversampling ratio OSR is given by,

$$OSR = \frac{F_S}{2B_S}$$

OSR = 100 MHz/(2x 200 KHz)

OSR = 250.

$$N \geq \left(\max\{-13-(-101), 0\} + 6 - 4.77 + 10Log_{10}\eta - 10Log_{10}OSR\right) \Big/ 6.02$$

N≥11.33

Therefore number of Bits is

N=12 bits.

To ensure proper operation, both over-ranging and under-ranging should be avoided. The over-ranging can be avoided by ensuring that the total power input to the ADC, $P_{T,}$ is less than the maximum power the ADC can quantize without clipping, $ADC_{max.}$.

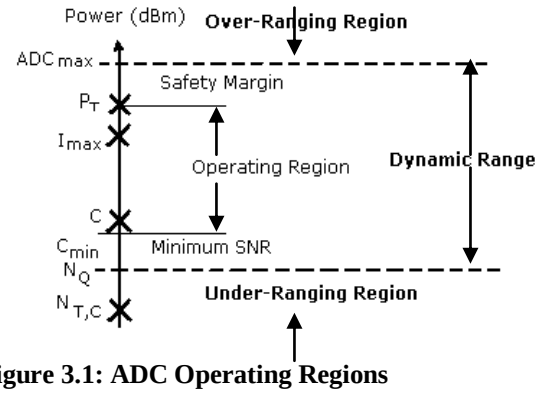

Figure 3.1: ADC Operating Regions

Quantization noise (N_Q) for number of bits, N=12 and the maximum ADC power,
ADC_{max} =2dBm

$$N_Q = \frac{V_{FS}^2}{2 \times 2^{2N}}$$

N_Q = - 95 dBm

This shows that ADC works in under ranging region for number of bits N=12 bits.
When C is less than $C_{min,}$ a gain stage can be used to shift C to proper level. The addition of gain G has the effect of shifting all the operating points, C, $P_{T,}$ and I_{max} up the power axis by G.
The maximum gain, G can added is calculated as

$$G \le ADC_{\max} - S.M. - P_T$$

Where ADC_{max} Maximum ADC Power, S.M. is Safety Margin, P_T Total signals Power.
For ADC_{max} = 2 dBm, S.M. = 9 dB, P_T = -13 dBm

G = 5 dB.

If this gain is too small to move C above $C_{min,}$ an ADC with a wider dynamic range must be required.
The number of bits N for added gain G can be calculated as

$$N \ge \left(ADC_{\max} - G - C + SNR_{\min} - 4.77 + 10Log_{10}\eta - 10Log_{10}OSR\right) \Big/ 6.02$$

The increased dynamic range can make Quantization Noise N_Q smaller than the Thermal Noise $N_{T,C.}$

$$N \ge \left(2 - 5 - (-101) + 6 - 4.77 + 10Log_{10}2 - 10Log_{10}250\right) \Big/ 6.02$$

N ≥ 13.1045
Therefore the number of bits N is
N = 14.
For N = 14 bits the Quantization Noise (N_Q) can be calculated.
The Quantization Noise (N_Q) = -107 dB.
The channel noise input to the radio at N=12 bits is given as the addition of Quantization Noise (N_Q) and maximum interference strength I_{max} is equal to **-118 dB.** The addition of gain G = 5 dB makes the Thermal Noise **$N_{T,C}$ = -113 dB at N = 14 bits.** Since the Thermal Noise $N_{T,C}$ is less than Quantization Noise (N_Q); this way the Quantization Noise may be colored.

3.3 Model Development of 14 bits Pipelined ADC:

The 4-stage pipelined Analog to Digital converter is shown in Figure 3.2. In operation, each stage initially samples and holds the output from the previous stage. Each stage then performs a low-resolution A/D conversion on the held input, and the code produced is converted back into an analog signal by a D/A converter. Finally the D/A converter output is subtracted from the held input, producing a residue that is amplified and sent to the next stage. All the digital outputs from each stage are combined and which give a final digital binary output code.
At any time, the first stage operates on the most recent sample, while the next stage operates on the residue from the previous sample, and so forth.

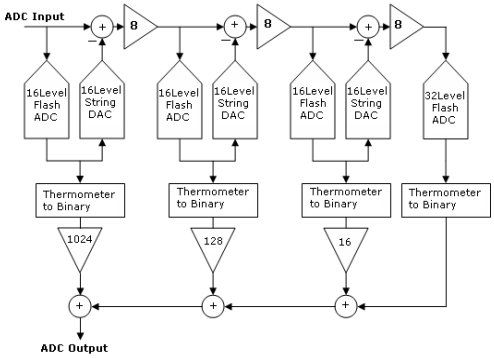

Figure 3.2. Functional diagram of the 14-bit four-stage pipelined ADC

The first three stages each incorporate a 16-level flash ADC and a 16-level string DAC, and the fourth stage consists of a 32-level flash ADC. The output of each 16-level ADC is the set of its 16 1-bit comparators outputs, and that of the 32-level ADC is the set of its 1-bit comparators outputs. This type of digital encoding is referred to as thermometer encoding, and the digital value of each ADC output is interpreted as the number of its comparator outputs that are high.
In each stage except for the last, the difference between the ADC input and DAC output is amplified by an interstage gain of 8.
Prior to arithmetic processing, the output of each ADC is converted from thermometer encoded data to binary encoded data $Dout(i)$ where i indicates the stage (i =1, 2, 3, 4). After the conversion, the digital signals from the ADCs are scaled and added to have digital output.

3.4 The Digital Correction and Output of the ADC: The difference between the analog input of the pipelined stage, which is the input of the sub ADC, and the DAC output of the same stage is referred as the residue. The transfer function from the input of the stage to the output of the subtractor is sawtooth shaped with the amplitude

$$FS / 2(Qi - 1) \quad \text{i = 1, 2, 3.}$$

where the input signal of each sub ADC ranges from –FS/2 and +FS/2 as for the total pipelined ADC. The number of bit n_i in stage i, then Qi is the number of output codes of the sub ADC in stage i, is equal to 16. The swing of the residue is thus 2^{ni} times smaller than the swing of the input signal to the next

stage and it is necessary to amplify the residue in order to utilize the entire swing of the following stage. By choosing the gain in the stage as Gi = 2^{ni} makes the swing equal to the FS of the following stage.

The digital outputs Dout (i) of the stages must be combined to generate the total output code of the pipeline converter. The output signal of the first stage is the input signal to the second stage. Hence each segment of the sawtooth shaped output signal of the first stage will be quantized by the second stage. It can be shown in figure 3.3. The total number of bits for the m stages is given by

$$N = \sum_{i=1}^{m} n_i$$

while Dout, the total digital output is,

$$D_{out} = \sum_{i=1}^{m} \left(D_{out}(i) . \prod_{k=i+1}^{m} 2^{nk} \right)$$

The four stage pipelined converter with the stage resolutions n1=n2=n3=4 and n4 = 5 bits. Therefore the gain for each stage is G1 = G2 = G3 = 16, then we get n = 17 and

$$D_{out} = 2^{n2}.2^{n3}.2^{n4}.D_{out}(1) + 2^{n3}.2^{n4}.D_{out}(2) + 2^{n4}.D_{out}(3) + D_{out}(4)$$

$$D_{out} = 8192.D_{out}(1) + 256.D_{out}(2) + 32.D_{out}(3) + D_{out}(4)$$

.This is not the case here that, the digital error correction (DEC) is extensively applied to relax the requirements of the comparators. In fact, in a pipelined converter where Gi=2^{ni}, the decision levels in the sub ADCs, and thereby also the comparators, must be very accurate if the total resolution of the converter is high. If a decision level in a sub-ADC is moved the stage output signal swing becomes larger than FS and the following sub-ADC will be overloaded and will saturate. Hence there is a large conversion error and the effective resolution of the converter is reduced.

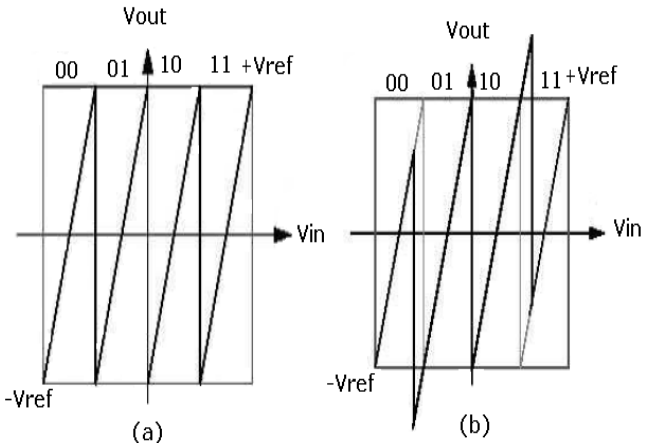

Figure 3.3: The digital output with respect to the input voltage Vin, (a) Transfer characteristic of a 2-bit stage from the input to the amplifier output in the ideal case (b) with errors affecting the decision levels of the sub-ADC.

The figure 3.3 shows transfer function characteristics of digital output versus input voltage. Here Vin is the input of a 2-bit stage; Vout is the output of the amplifier and represents the amplified residue. For the FS/2 = Vref, so that input signal of the sub ADC ranges from -Vref and +Vref. The transfer function from the input of the stage to the output of the subtractor is sawtooth shaped. In order to utilize the entire swing of the following stage, which is equal to the first one, it is necessary to amplify the residue. Choosing the gain in the stages as G = 4 makes the swing equal to 2.Vref, that is the full scale (FS) of the following stage. This reasoning could be easily applied if the system was ideal and, in particular if there were no errors affecting sub-DAC decision levels. But, in a flash ADC, the decision levels depend on the thresholds of the comparators, which are subject to fluctuations because of non-idealities. The figure 3.3 (b) shows error affecting the decision levels; which move the residue output swing larger than the Vref=4. Therefore, if amplification is not reduced, the sub-ADC of the next stage will be overloaded.

To solve this problem, in a pipelined ADC with digital correction, the residue gain is reduced and the output of the following stages is digitally corrected to compensate the reduced gain. Therefore the residue gain has been reduced from 16 to 8. The outputs signal swing of the first, a second and third stage is only one half the input range of the following stages: this means that some of the codes in the second, third and fourth ADC will never be used. This is why the total resolution is 14 bits and not 17 as we calculated before without taking into account the digital correction. All the codes in the first stage are used.

The outputs of all stages are digitally corrected except last stage, and the residue gain of all stages, apart from the last, for which it is not necessary to generate the residue, are reduced. The bit redundancy is introduced in all stages, apart from the first stage. The xi number of bits used by the i-th stage for digital correction, then the effective resolution of the respective stage is $n_{eff,i} = n_i - x_i$ and the total number of effective output bits can be given as

$$N = \sum_{i=1}^{m} ne_{ff,i}$$

Parameter	**1st Stage**	**2nd stage**	**3rd stage**	**4th stage**
n_i	**4**	**4**	**4**	**5**
x_i	**0**	**1**	**1**	**1**
$n_{eff,i}$	**4**	**3**	**3**	**4**
Q_i	**16**	**16**	**16**	**32**
Gi	**8**	**8**	**8**	**-**

The various parameters of 14-bit pipelined ADC are given in table 3.3.

Table 3.3: Parameters of Pipelined ADC.

It is desirable that to have the same step size for all the codes in the following sub-ADC and the gain is then restricted to values that give the correct step size at the decision levels in the first stage. The digital correction can correct errors in the comparators as long as the residue is within the FS range of the following stage. The smaller the residue gain, the larger errors can be accepted. The maximum decision level deviation allowed without large conversion errors is given by

$$\Delta V = \pm \frac{FS}{2}\left(\frac{1}{Gi} - \frac{1}{2^{n_i}}\right)$$

The Digital Output of Pipelined ADC is given as

$$Dout = \sum_{i=1}^{m}\left(D_{out}(i).\frac{2^{n_m}}{2^{n_i}}.\prod_{k=i}^{m-1}G_k\right)$$

$$Dout = \frac{2^{n_4}}{2^{n_1}}G1G2G3D_{out}(1) + \frac{2^{n_4}}{2^{n_2}}G2G3D_{out}(2) + \frac{2^{n_4}}{2^{n_3}}G3D_{out}(3) + D_{out}(4)$$

$$Dout = 1024.Dout(1) + 128.Dout(2) + 16.Dout(3) + Dout(4)$$

It is easy to verify that in this case the digital codes from the stages overlap when they are added and digital logic must handle carry propagation in the addition. In this way the output of pipelined ADC results has a 14-bit resolution.

4. RESULTS AND DISCUSSION:

The 14-Bit Pipelined ADC is modeled in respect of GSM – 900 systems for Software Defined Radio. The number of bits of ADC depends on the various practical parameters.

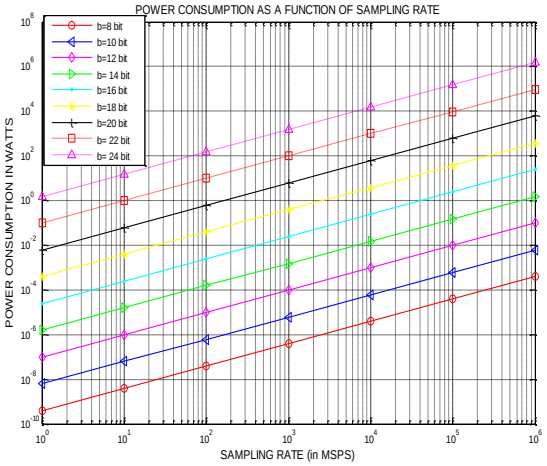

Figure 4.1: Minimum Power Consumption as a Function of sampling Rate for various resolutions

For the ADC to fully utilize the available resolution, its quantization noise power should be less than the thermal noise power at the input of ADC. The minimum power consumed is depend on the sampling rate and the number of quantization bits is shown in figure 4.1.
The 14- bits ADC require around 4x 10^{-4} of power at 100 MHz sampling rate.

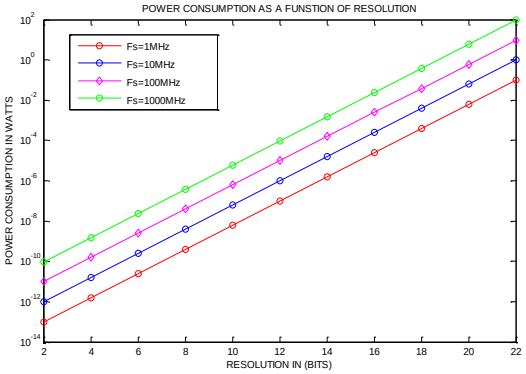

Figure 4.2: Minimum Power Consumption as a Function of Resolution for various Sampling Rate

The relationship between minimum power consumption and the number of quantization bits for a number of different sampling rates is shown in figure 4.2 The minimum power consumed is depend on the sampling rate and the number of quantization bits. The 14-bit resolution ADC requires 1mW of power at 1 GSPS.

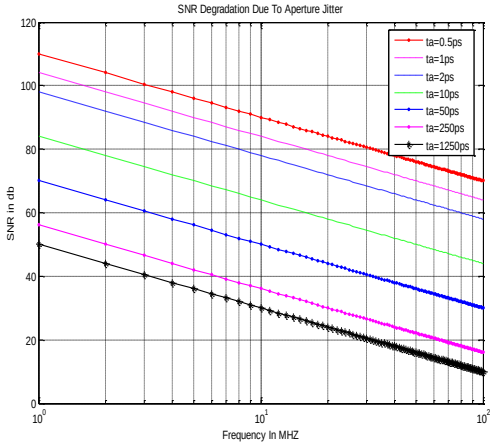

Figure 4.3: SNR Degradation Due to Aperture Jitter
The Signal to Noise Ratio decreases as the aperture jitter increases for the input frequency signal is shown in figure 4.3.

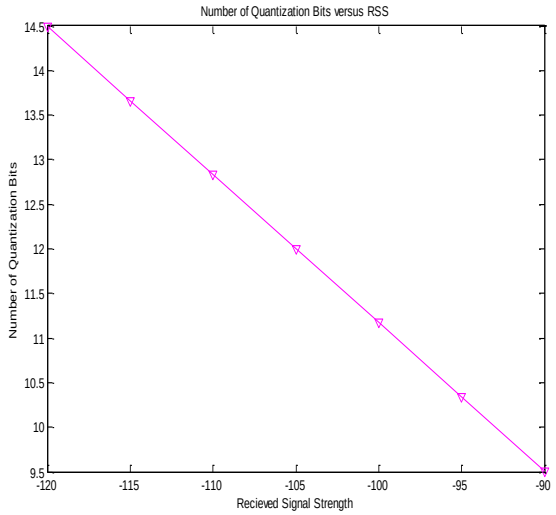

Figure 4.4: Number of Quantization bit as a function RSS

The number of quantization bits for ADC increases as the strength of the received signal decreases is shown in figure 4.4. The RSS is related to the resolution by the dynamic range of an ADC.

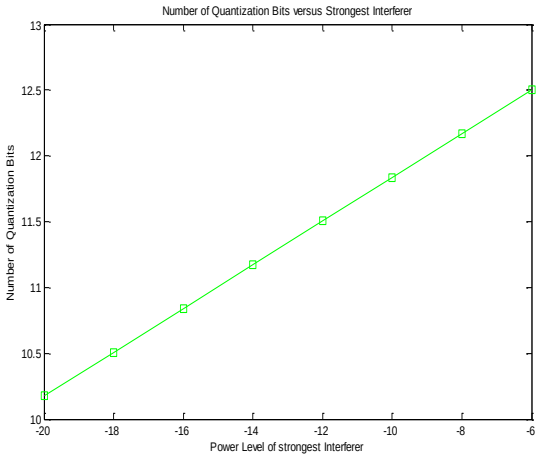

Figure 4.5: Number of Quantization bit as a function of Interference

The number of quantization bits for ADC increases as the level of interferer increases is shown in figure 4.5. To receive the signal successfully in the presence of the strong interferer which is present in the noisy environment; the ADC should have sufficient resolution.

The table 4.1 shows the binary output of the 14-bit pipelined ADC for various analog input sample values. This shows the monotonic relationship between analog input sample values and the binary output.

Sr. No.	**Analog Input Sample Value (Vin)**	**Pipelined ADC 14-Bits Output (Dout)**
01	1.235	1 0 0 1 1 1 0 0 0 1 1 0 0 0
02	0.0873	0 0 0 0 0 1 1 0 1 0 1 0 0 0
03	0.0920	0 0 0 0 0 1 1 1 0 0 1 1 0 0
04	1.6500	1 1 0 1 0 1 1 0 1 1 0 1 0 1
05	1.9000	1 1 1 1 0 1 1 0 1 1 0 1 0 1

TABLE 4.1

5. C0NCLUSION:

In future ,terminals will become ‘’future proof”within limitations of terminal’s hardware by having the capability to download new air interfaces, and operate on new communications standards,using lower layer reconfigurations technology implemented with software radio technology.The ADC has been modeled in MATLAB software obeying the given constraints.

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